CHAPTER ELEVEN - Interfacing With the Analog World

11.1 (a) Analog output = (K) x (digital input)

(b) Smallest change that can occur in the analog output as a result of a change in the digital input.

(c) Same as (b).

(d) Maximum possible output value of a DAC.

(e) Ratio of the step size to the full-scale value of a DAC. Percentage resolution can also be defined as the reciprocal of the maximum number of steps of a DAC.

(f) False.

(g) False (It is the same).

11.2 01100100₂ = 100₁₀
    10110011₂ = 179₁₀
(179/100) = (X/2V)
X = 3.58V

11.3 LSB = 2V/100 = 20mV
    Other bits: 40mV, 80mV, 160mV, 320mV, 640mV, 1280mV, and 2560mV.

11.4 Resolution = Weight of LSB = 20mV; % Resolution = [1/(2^8-1)] x 100% ≈ 0.4%

11.5 10 bits ---> 2^{10}-1 = 1023 steps; Resolution = 5V/1023 ≈ 5mV

11.6 Assume resolution = 40µA. The number of steps required to produce 10mA F.S. = 10mA/40µA = 250. Therefore, it requires 8 bits.

11.7 Number of steps = 7; % Resolution = 1/7 = 14.3%; Step-size = 2V/7 = 0.286V

11.8 The glitches are caused by the temporary states of the counter as FFs change in response to clock.

11.9 12-bit DAC gives us 2^{12}-1 steps = 4095. Step-Size = F.S/# of steps = 2mA/4095 = 488.4nA
    To have exactly 250 RPM the output of the DAC must be 500µA. ((250 x 2mA)/1000RPM)
    In order to have 500µA at the output of the DAC, the computer must increment the input of the DAC to the count of 1023.75. (500µA/488.4nA)
    Thus, the motor will rotate at 250.061 RPM when the computer’s output has incremented 1024 steps.

11.10 Step Size (resolution) = V_{FS} / (2^{12} – 1) = 3.66 mV
    % Resolution = step size / full scale x 100% = 3.66 mV / 15.0 V x 100% = 0.024%
    011010010101₂ = 1685₁₀
    Vout = 1685 x 15 / 4095 = 6.17 V

11.11 The most significant 8 bits: DAC[9..2] => PORT[7..0].
    Full scale is still 10 volts and step size is 39 mV.
11.12 Number of steps = 12 V / 20mV = 600
2^n – 1 > 600, Thus, n = 10 bits.

11.13 (a) Step-Size = R_F x (5V/8KΩ) = 0.5V. Therefore, R_F = 800Ω
(b) No. Percentage resolution is independent of R_F.

11.14 (a) I_O = V_{REF}/R = 250µA
LSB = I_O/8 = 31.25µA
V_{OUT(LSB)} = -31.25µA x 10KΩ = -0.3125V
V_{OUT(Full Scale)} = -10KΩ(31.25+62.5+125+250)µA = -4.6875V
(b) (-2V/-4.6875V) = R_F/10KΩ
R_F = 4.27KΩ
(c) V_{OUT} = K(V_{REF} x B)
-2V = K(5V x 15)
K = -0.0267

11.15 With the current IC fabrication technology, it is very difficult to produce resistance values over a wide resistance range. Thus, this would be the disadvantage of the circuit of figure 11.7, especially if it was to have a large number of inputs.

11.16 (a) Absolute error = 0.2% x 10mA = 20µA
(b) Step-Size = (F.S./# of steps) = 10mA/255 = 39.2µA. Ideal output for 00000001_2 is 39.2µA. The possible range is 39.2µA ± 20µA = 19.2µA - 59.2µA. Thus, 50µA is within this range.

11.17 (a) 0.1 inches out of a total of 10 inches is a percentage resolution of 1%. Thus, (1/2^n-1) x 100% <1%. The smallest integer value of n which satisfies this criteria is n=7.
(b) The potentiometer will not give a smoothly changing value of V_P but will change in small jumps due to the granularity of the material used as the resistance.

11.18 (a) Resistor network used in simple DAC using a an op-amp summing amplifier. Starting with the MSB resistor, the resistor values increase by a factor of 2.
(b) Type of DAC where its internal resistance values only span a range of 2 to 1.
(c) Amount of time that it takes the output of a DAC to go from zero to within 1/2 step size of its full-scale value as the input is changed from all 0s to all 1s.
(d) Term used by some DAC manufacturers to specify the accuracy of a DAC. It's defined as the maximum deviation of a DAC's output from its expected ideal value.
(e) Under ideal conditions the output of a DAC should be zero volts when the input is all 0s. In reality, there is a very small output voltage for this situation. This deviation from the ideal zero volts is called the offset error.
11.19 Step-Size = 1.26V/63 = 20mV; ±0.1% F.S. = ±1.26mV = ±1mV
Thus, maximum error will be ±2.26 mV.

<table>
<thead>
<tr>
<th>Binary</th>
<th>Value (mV)</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>000010₂</td>
<td>2 x 20mV = 40mV</td>
<td>[41.5mV is within specs.]</td>
</tr>
<tr>
<td>001111₂</td>
<td>7 x 20mV = 140mV</td>
<td>[140.2mV is within specs.]</td>
</tr>
<tr>
<td>000110₀₂</td>
<td>12 x 20mV = 240mV</td>
<td>[242.5mV isn't within specs.]</td>
</tr>
<tr>
<td>111111₀₂</td>
<td>63 x 20mV = 1.26V</td>
<td>[1.258 V is within specs.]</td>
</tr>
</tbody>
</table>

11.20 The actual offset voltage is greater than 2mV. In fact, it appears to be around 8mV.

11.21 The DAC’s binary input next to the LSB (00000000) is always HIGH. It is probably open.

11.22 The graph of Figure 11.32 would've resulted, if the two least significant inputs of the DAC were reversed (00000000₂). Thus, the staircase would've incremented in the following sequence: 0,2,1,3,4,6,5,7,8,10,9,11,12,14,13,15.

11.23 A START pulse is applied to reset the counter and to keep pulses from passing through the AND gate into the counter. At this point, the DAC output, \( V_{AX} \), is zero and \( \overline{EOC} \) is high. When START returns low, the AND gate is enabled, and the counter is allowed to count. The \( V_{AX} \) signal is increased one step at a time until it exceeds \( V_A \). At that point, \( \overline{EOC} \) goes LOW to prevent further pulses from being counted. This signals the end of conversion, and the digital equivalent of \( V_A \) is present at the counter output.

11.24 (a) \((\)Digital value\( ) \times (\)resolution\( )) \geq V_A +V_T; \ (\)Digital value\( ) \times (40\)m\( V) \geq 6.001\)V = 6001m\( V\). Therefore, Digital value \( \geq 150.025\). This indicates a digital value of 151 or written in binary 10010111₂.

(b) Using same method as in (a) the digital value is again 10010111₂.

(c) Maximum conversion time = \((\)max. \# of steps\( ) \times (\)T\_CLOCK\( )\); \( T\_CLOCK = (2^8-1) \times (0.4\)µs\( ) = 102\)µs. Average conversion time = \( 102\)µs/2 = 51µs.

11.25 Because the difference in the two values of \( V_A \) was smaller than the resolution of the converter.

11.26 The A/D converter has a full-scale value of \((2^8-1) \times 40\)m\( V\) = 10.2V. Thus, a \( V_A \) of 10.853V would mean that the comparator output would never switch LOW. The counter would keep counting indefinitely producing the waveform below at the D/A output.
The circuit below can be used to indicate an over-scale condition.

![Circuit Diagram]

11.27  (a) With 12 bits, percentage resolution is \(1/(2^{12}-1)\) x 100% = 0.024%. Thus, quantization error = 0.024% x 5V = 1.2mV.

(b) Error due to .03% inaccuracy = .03% x 5V = 1.5mV. Total Error = 1.2mV + 1.5mV = 2.7mV.

11.28  (a) With \(V_A = 5.022\)V, the value of \(V_{AY}\) must equal or exceed 5.023V to switch COMP. Thus, \(V_{AX}\) must equal or exceed 5.018V. This requires 5.018V/10mV = 501.8 = 502 steps.

This gives \(V_{AX} = 5.02\)V and digital value 0111110110\(_2\).

(b) \(V_{AY} \geq 5.029\)V, \(V_{AX} \geq 5.024\)V; # of steps = 5.024V/10mV = 502.4 = 503 steps (\(V_{AX} = 5.03\)V). This gives digital value 0111110111\(_2\).

(c) In (a) quantization error is \(V_{AX} - V_A = 5.02\)V - 5.022V = -2mV. In (b) \(V_{AX} - V_A = 5.03\)V - 5.028V = +2mV

11.29 0100011100\(_2\) = 284\(_{10}\); At count of 284\(_{10}\), \(V_{AY} = 2.84\)V + 5mV = 2.845V; At count of 283\(_{10}\), \(V_{AY} = 2.83\)V + 5mV = 2.835V. Thus, the range of \(V_A = 2.8341\)V --> 2.844V

11.30

![Waveform Graph]

V vs Time

1v/25us
For a more accurate reproduction of the signal, we must have an A/D converter with much shorter conversion times. An increase in the number of bits of the converter will also help, especially during those times when the original waveform changes rapidly.

11.31

![Diagram](image)

(a) Since the Flash ADC samples at intervals of 75µs, the sample frequency is \(1/75\mu s = 13.33\) kHz.

(b) The sine wave has a period of 100 µs or a \(F = 10\) kHz. Therefore, the difference between the sample frequency and the input sine wave frequency is 3.3 kHz.

(c) The frequency of the reconstructed waveform is approximately \(1/300\) µs or 3.33 kHz.

11.32

(a) Input signal = 5 kHz; (b) Input signal = 9.9 kHz; (c) Input signal = 9.8 kHz

(d) Input signal = 5 kHz; (e) Input signal = 900 Hz; (f) Input signal = 800 Hz

11.33

(a) digital-ramp ADC; (b) successive approximation ADC; (c) successive approximation ADC

(d) both; (e) both; (f) digital-ramp ADC; (g) successive approximation ADC; (h) both

11.34
11.35

\[ V_{\text{AX}} (\text{V}) \]

\[ 15 \]

\[ 14 \]

\[ 12 \]

\[ 8 \]

\[ 0 \]

\[ t_0 \]

\[ t_1 \]

\[ t_2 \]

\[ t_3 \]

\[ t_4 \]

\[ \text{Time} \]

11.36 80µs: Conversion time is independent of \( V_A \).

11.37 \( t_0 \): Set MSB (bit 5);  \( t_1 \): Set bit 4; clear bit 4;  \( t_2 \): Set bit 3; clear bit 3;  \( t_3 \): Set bit 2  \( t_4 \): Set bit 1; clear bit 1;  \( t_5 \): Set LSB;  Digital result = 100101_2

11.38 The range is 3.0V; The offset is 0.5V.; The Resolution = 3V/255 = 11.76mV; 10010111_2 = 151_{10}
Thus, the value of the analog input is approximately \((151_{10} \times 11.76\text{mV}) + 0.5\text{V} = 2.276\text{V}\)

11.39 With \( V_{\text{REF}}/2 = 2.0\text{V} \), the range is = 4V; The offset is 0.5V.
The Resolution = 4V/255 = 15.69mV; 10010111_2 = 151_{10}. Thus, the value of the analog input is approximately \((151_{10} \times 15.69\text{mV}) + 0.5\text{V} = 2.869\text{V}\)

11.40 (a) Since we must measure accurately from 50°F to 101°F, the digital value for 50°F for the best resolution should be 00000000_2.

(b) The voltage applied to the input \( V_{\text{IN}}(\cdot) \) should be 500mV. With \( V_{\text{IN}}(\cdot) = 500\text{mV} \), when the temperature is 50°F the ADC output will be 00000000_2.

(c) The full range of voltage that will come in is: \((101^\circ\text{F} \times 0.01\text{V}) - (50^\circ\text{F} \times 0.01\text{V}) = 510\text{mV}\).

(d) A voltage of 255mV (full range/2) should be applied to \( V_{\text{REF}}/2 \) input.

(e) An input temperature of 72°F causes the LM34 sensor to output a voltage of \((72^\circ\text{F} \times 0.01\text{V}) = 720\text{mV}\). However, since there is an offset voltage of 500mV, the ADC will convert \((720\text{mV} - 500\text{mV}) = 220\text{mV}\). The resolution will be 510mV/256 = 1.99mV, so 220mV/1.99mV = 110_{10} = 01101110_2.

(f) The sensor will change by 10mV for every 1°F change. Therefore, an output change of one step of the ADC (1.99mV) corresponds to a temperature change of 0.199°F. Thus, the resolution is 0.199°F/step.
11.41 Since a conversion would take place every 1µs rather than the 1V/25µs rate of conversion, the result would've been a much closer reproduction of the analog signal.

11.42

11.43 (a) flash. (b) digital-ramp and SAC; (c) flash. (d) flash; (e) digital-ramp. (f) digital-ramp, SAC, and flash; (g) SAC and flash.
11.44  (a) pipelined  
       (b) flash ADC  
       (c) voltage-to-frequency ADC  
       (d) voltage-to-frequency ADC  
       (e) dual-slope ADC  
       (f) dual-slope ADC.

11.45  If the switch is stuck closed, the output will follow $V_A$. If the switch is stuck open, or if $C_h$ is shorted, the output will be 0V.

11.46  

A MOD-16 counter is used between the 50KHz clock and the clock input of the MOD-4 counter because a 320µs time delay is needed for the proper operation of the circuit. The 320µs was determined according to the following requirements:

(a) 200µs for the time conversion (10-bits x clock period).

(b) The outputs must remain stable for 100µs after the conversion is complete.

(c) A 10µs delay (OS1) is needed in order to allow the analog signal $V_A$ to stabilize before the ADC is given a Start pulse.

(d) Finally, a 10µs-duration Start pulse is required (OS2).

11.47  (a) The $\overline{CS}$ signal is LOW only when ALE=0 and the following address is on the address bus:

<table>
<thead>
<tr>
<th>A15</th>
<th>A14</th>
<th>A13</th>
<th>A12</th>
<th>A11</th>
<th>A10</th>
<th>A9</th>
<th>A8</th>
<th>A7---&gt;A0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>x---&gt;x</td>
</tr>
</tbody>
</table>

$x_{16} = EAXX_{16}$
(b) Add an inverter between address line A9 and input A1 of the 74LS138.
(c) 1. Remove the inverter between address line A12 and the NAND gate.
2. Change $\overline{CS}$ from output 2 of the 74LS138 to output 7.

11.48 Yes. Connect the two least significant bits (b0 and b1) to ground. Attach b2 through b9 from the ADC to the port.

11.49

<table>
<thead>
<tr>
<th>Sample</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN[n] (v)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>OUT[n] (v)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2.5</td>
<td>5</td>
<td>7.5</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

11.50

<table>
<thead>
<tr>
<th>Sample</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN[n] (v)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>OUT[n] (v)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>7</td>
<td>9</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

11.51 Multiply Accumulate

11.52 (a) F (b) T (c) T (d) T (e) F (f) T (g) F (h) T