Lecture 1

Wafer fabrication and Silicon epitaxy
Silicon wafer fabrication
Wafer fabrication

Starting material: Electronically-grade Si (EGS) with contamination below ppb level

Czochralski method

Loading the high purity poly-Si

Silicon Ingot

Seed Down  Seed Pulling  Shoulder  Si Crystal Growth
Standard for CMOS.

Dash method for moving dislocations out from the surface at the pulling seed.


Dopant incorporation: Segregation coefficient $k_0 = \frac{C_{\text{Solid}}}{C_{\text{liquid}}}$

(Plummer Fig. 3.18 p 128)
**Float-zone method**

No crucible, crystal formed in Ar atmosphere

Low oxygen content

High-resistivity possible

Neutron Transmutation Doping for extremely high-uniform resistivity

Difficult to scale up in wafer diameter
Defects in Si

Point defects:

V vacancy (neutral, single- or double-charged)  
(see further Plummer p133-138)

I interstitial or interstitialcy

1-D defect: dislocation

2-D defect: Stacking fault

3-D defect: Precipitates  
(oxygen precipitation)

Figure 3-4 Simple 2D representation of some of the common defects found in crystals. V and I are point defects, the edge dislocation represents a typical line defect, the stacking fault is an area defect, and the precipitate is a volume defect.

(Plummer Fig. 3-4 p 98)
Oxygen in CZ-Si

Oxygen dissolves from quartz crucible during CZ growth

$\sim 10^{18} \text{ cm}^{-3}$

Three effects during circuit processing:

+ Si-O-Si bindings resulting in higher mechanical strength

- Oxygen donors ($\text{SiO}_4$). $10^{16} \text{ cm}^{-3}$ form at 400-500°C

- Bulk precipitation ($\text{SiO}_2$) (but can be controlled by gettering)
**SOI: Silicon-on-insulator wafers**

Buried oxide layer $\sim 10^3$ Å thick

SIMOX: Separation by implanted oxygen (SIMOX)

BESOI: Bonded and etch-back technology (BESOI)

Smart-cut: H implant before BESOI process

SOS wafers: Silicon-on-sapphire
Gettering

Capture defects at locations far away from the device region.

Damaged region will act as "sink" for unwanted elements.
**Extrinsic gettering:**
Treatment on backside of wafer, e.g. n⁺ doping

**Intrinsic gettering:**
Intentional SiO₂ precipitation inside bulk.
Requires dedicated thermal cycling:

(Plummer Fig 4-12)
Outline:
- Definition and terminology
- Chemical vapor deposition
- CVD process and source gases
- Grove model:
  - Mass-transfer or surface-reaction controlled growth rate
- Gas flow and pressure in CVD
- Chlorine in Si CVD
- Doping
  - Autodoping
- Defects and characterization
- Reactor types
  - Batch
  - Single-wafer
  - MBE
- Applications of Si epitaxy
  - HT epitaxy: Si
  - LT epitaxy: SiGe
  - Selective epitaxy: Si and SiGe
Book references cited:

S.M. Sze: Semiconductor Devices 1985
S-M.Sze ed: VLSI Technology 1988
Chang and S.M. Sze: ULSI Technology 1996
S. Wolf and R.N. Tauber: Silicon Processing for VLSI vol. 1 1986
J. Plummer, Silicon VLSI Technology 2000
**Silicon epitaxy**

**Definition**

Growth of single-crystalline layer on a single-crystalline substrate (bulk)

Epitaxial layer thickness: From one single atom layer up to ca 100 µm

**Homoepitaxy**: Si on Si  
**Heteroepitaxy**: e.g. SixGe1-x on Si

Doping level can vary substantially between the layer and bulk

**Advantages with epitaxy:**

- Lower temperature compared to implantation + diffusion → much more abrupt doping profiles
- Large interval of thicknesses, doping profiles, and band gap engineering → ideal for creating "artificial" semiconductor structures, e.g. HBTs, HEMTs
Silicon epitaxy:

Conventional, or high-temperature (HT), epitaxy at $T > 1000^\circ \text{C}$
(on blanket or patterned wafers)

Low-temperature (LT or LTE) epitaxy at $T < 1000^\circ \text{C}$.
(Usually on patterned substrates)

Selective epitaxy (always on patterned substrates)

Terminology for CVD SiGe epitaxy:

Selective epitaxial growth: SEG

Non-selective epitaxial growth: NSEG
Heteroepitaxy (SiGe on Si)

Strained growth conditions, so-called pseudomorphic growth

$h_c = \text{critical thickness}$

Unstrained $\rightarrow$ dislocation network which are adverse for device operation

**FIGURE 1**
Schematic drawings of typical (a) unstrained and (b) strained heteroepitaxy.

(Chang p.106)
Technology of choice for Si epitaxial growth in production environment:

Chemical vapor deposition (CVD)
(sometimes denoted vapor phase epitaxy (VPE))

Hydrogen ($H_2$) carrier gas
Reactants: $SiCl_4$, $SiHCl_3$, $SiH_4$, + dopant gases ($AsH_3$, $B_2H_6$...)
$HCl$ for selective growth and/or chamber cleaning
$N_2$ for purge

**FIGURE 2**
Schematic illustration of a typical VPE process.
Basic Si CVD types (both batch and single-wafer reactors)

**APCVD** (atmospheric pressure CVD)
Only for HT epitaxy (e.g. p-epitaxy on p+ bulk)

**LPCVD** (low-pressure CVD)
Deposition around 10-100 torr, e.g. for n+ HT epitaxy, LT SiGe epitaxy or SEG

**UHVCVD** (ultra-high vacuum CVD)
Deposition around 10-3 torr. For LT SiGe epitaxy (NSEG)
CVD process

1. Transport of reactants to the deposition region
2. Transport of reactants by diffusion from the main gas stream through the boundary layer to the wafer surface
3. Adsorption of reactants on the wafer surface
4. Surface processes: migration, decomposition, reaction, site incorporation
5. Desorption of byproducts from surface
6. Transport of byproducts through the boundary layer
7. Transport of byproducts from the deposition region

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**Figure 9-5** Steps involved in a CVD process. Numbered steps are explained in text.

(Plummer Fig 9-5 p 514)
Si CVD sources and basic reactions for HT epitaxy

Silicon tetrachloride: \[ \text{SiCl}_4 + \text{H}_2 \leftrightarrow \text{Si} + 4\text{HCl} \quad (~1200^\circ\text{C}) \]

Trichlorosilane (TCS): \[ \text{SiHCl}_3 + \text{H}_2 \leftrightarrow \text{Si} + 3\text{HCl} \quad (~1150^\circ\text{C}) \]

Dichlorosilane (DCS): \[ \text{SiHCl}_2 \leftrightarrow \text{Si} + 2\text{HCl} \quad (~1100^\circ\text{C}) \]

Silane: \[ \text{SiH}_4 \rightarrow \text{Si} + 2\text{H}_2 \quad (~1050^\circ\text{C}) \]

HT epitaxy: TCS or DCS
LT epitaxy: DCS or silane

<table>
<thead>
<tr>
<th>Chemical deposition</th>
<th>Nominal growth rate(μm/min)</th>
<th>Temperature range(°C)</th>
<th>Allowed oxidizer level (ppm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>\text{SiCl}_4</td>
<td>0.4–1.5</td>
<td>1150–1250</td>
<td>5–10</td>
</tr>
<tr>
<td>\text{SiHCl}_3</td>
<td>0.4–2.0</td>
<td>1100–1200</td>
<td>5–10</td>
</tr>
<tr>
<td>\text{SiH}_2\text{Cl}_2</td>
<td>0.2–1</td>
<td>1050–1120</td>
<td>&lt;5</td>
</tr>
<tr>
<td>\text{SiH}_4</td>
<td>0.2–0.3</td>
<td>950–1250</td>
<td>&lt;2</td>
</tr>
</tbody>
</table>

(Sze VLSI Table I p. 65)
The Grove model for epitaxial growth

Growth limited by mass-transfer or surface reaction

\[ F_1 = h_g \left( C_g - C_s \right) \]
\[ F_2 = k_s C_s \]

- \( h_g \): vapor mass transfer coefficient
- \( k_s \): surface reaction constant

Assume:

- Steady state: \( F_1 = F_2 = F \)
- Growth rate: \( n = F/C_a \) where \( C_a \) = number of Si atoms/cm³

\( C_g = yC_t \) where \( y \) is the mole fraction and \( C_t \) is the total number of gas molec/cm³

\[ v = \frac{k_s h_g}{k_s + h_g} \left( \frac{C_t}{C_a} \right) y \]

- When \( k_s \) is small \( \Rightarrow \) Surface reaction controlled: \( v \approx k_s \left( \frac{C_t}{C_a} \right) y \)
- When \( h_g \) is small \( \Rightarrow \) Mass-transport controlled: \( v \approx h_g \left( \frac{C_t}{C_a} \right) y \)
Consequences:

Figure 9-7 Arrhenius plot of growth velocity (or deposition rate) vs. $1/T$ for CVD process. The net growth velocity is the result of the surface reaction and gas-phase mass transfer processes acting in series so that the slower of the two dominates at any temperature.

(Szems Fig 9-7)

Fig. 21 Temperature dependence of the growth rate for various silicon sources.¹³

(Sze Fig 21 p. 326)
Gas flow rate
Mass-transport controlled regime

Laminar gas flow with velocity $v$ above a boundary layer with thickness $\delta$

Analysis of friction force $\Rightarrow h_g = D_g / d \sim \sqrt{v}$
where $D_g$ is gas diffusion coefficient across $\delta$

(Sze Fig. 22 p. 327)

(Fig. 22) (a) Development of a boundary layer in gas flow over a flat plate. (b) Expanded view of the boundary layer.

(Chang Fig 7 p 114)
Surface reaction controlled regime:

Deposition not (very) sensitive to geometrical arrangement of wafers in reactor. However, low growth rates!

Can be solved by reducing total pressure which affects $D_G$ and extends surface-reaction limited region to higher $T$:

![Graph showing growth velocity vs. $1/T$ for APCVD (760 torr) and LPCVD (1 torr) systems. The lower total pressure (with $P_0$ and $C_0$ remaining fixed) shifts the $k_G$ curve upward, extending the surface reaction regime to higher temperatures.](Plummer Fig 9-13)
Si epi-growth rate for Cl-based chemistry

Either deposition or etching depending on T, P or concentration (mole Fraction)

Reaction is complex, e.g. SiCl$_4$:

\[
\begin{align*}
\text{SiCl}_4 + \text{H}_2 & \rightleftharpoons \text{SiHCl}_3 + \text{HCl} \\
\text{SiHCl}_3 + \text{H}_2 & \rightleftharpoons \text{SiH}_2\text{Cl}_2 + \text{HCl} \\
\text{SiH}_2\text{Cl}_2 & \rightleftharpoons \text{SiCl}_2 + \text{H}_2
\end{align*}
\]
Reversible reactions!

Crystallinity also depends on growth rate:

**Fig. 2** Silicon growth rate as a function of SiCl₄ concentration⁵². Reprinted with the permission of the publisher, the Electrochemical Society. (Sze p. 322)

**FIGURE 10**
Crystallinity with respect to growth rate and growth temperature. (After Bloom, Ref. 10.) (Chang Fig 10 p)
Doping in Si epitaxy

*Doping sources*: $\text{B}_2\text{H}_6$ (diborane), $\text{AsH}_3$ (arsine) and $\text{PH}_3$ (phosphine).
*Not* standard: $\text{SbCl}_5$

*Dopant incorporation* dependent upon T, growth rate, dopant/Si ratio in gas phase, reactor geometry

$\text{B}_2\text{H}_6$ enhances growth rate
$\text{PH}_3$ reduced growth rate

Example from KTH:
Double-epi ($n^-/n^+$) using $\text{AsH}_3$ on $p^-$ bulk

Radamson & Grahn 98
Autodoping

Lightly doped n-epi-layer grown on n+ substrate → autodoping, i.e. *unintentional doping from substrate, susceptor, adjacent wafers etc.*

Both *vertical* and *lateral* autodoping may occur, e.g. during epitaxy on buried n+-layer

Remedies:

- Low-pressure CVD for HT n-type epi
- Reduced deposition temperature

Observe: Autodoping is not a problem for B!
Defects in epitaxial layers

Dislocations (line defect)
Stacking faults (area defect) visible as squares for (100) and triangles for (111)
Precipitates (volume defect)
Hillocks or voids (volume defects)

Substrate surface quality and cleaning prior to epitaxy are crucial, in particular LT epitaxy.

*Slip* in HT epitaxy:
Dislocation network caused by temperature gradient across wafer during RTA-CVD (single-wafer machines)
Epi thin film characterization

Surface smoothness:
Optical microscopy
Nomarski contrast microscopy
Atomic force microscopy (AFM)

Film thickness and doping:
Secondary ion mass spectroscopy (SIMS)
Fourier-transform Infrared Spectroscopy (FTIR) (see below)

Crystallographic quality:
High-resolution X-ray diffractometry for Ge content and thickness in SiGe

Electrical properties:
Film resistivity vs doping
Minority carrier life time measurement
Device characteristic
Reactor types for Si epitaxy

Batch reactor types
Almost only for HT epitaxy (exception UHVCVD)

FIGURE 20
Types of conventional epitaxial reactors: (a) horizontal reactor; (b) vertical reactor; (c) barrel reactor. (After Pearce, Ref. 27.)

(Chang Fig. 20 p124)
Example of batch type epi-reactors:

Fig. 21 Schematic of an induction heated vertical pancake reactor. Courtesy of Microelectronic Manufacturing and Testing.

Fig. 22 Schematic of a radiantly heated barrel reactor. Courtesy of Applied Materials Inc.
Single-wafer Si epitaxy

RTP process!
Both for HT and LT epitaxy (Si/SiGe)
Used for production of wafers, epi on buried layers and LT epi SiGe.
Example:

Fig. 1 - Top view (a) and cross section (b) of the reactor chamber, showing the geometry and the position of the heating lamps with respect to the wafer, susceptor and thermocouples (t.c.).

(ASM Epsilon 2000 at KTH)
UHVCVD
LT non-selective epi method developed by IBM specially for SiGe
Batch method at very low temperature 500-600°C

FIGURE 22
Schematic drawing of a UHVCVD system. (After Meyerson, Ref. 29.)

(Chang Fig 22 p 128)
Special wafer cleaning developed, so-called hydrogen termination of Si surface using an HF dip prior to loading.
No *in situ* surface cleaning!

**FIGURE 21**
Water vapor pressure vs. reciprocal temperature for oxide-free and oxidized Si surfaces. *(After Meyerson, Ref. 29.)*

*(Chang Fig 23 p129)*
Silicon Molecular Beam Epitaxy (MBE)

Physical vapor deposition (PVD) method

Typical for thin film research for SiGe(C) epitaxy (not in production!)

- Vacuum evaporation with excellent thickness control
- Ultra-high vacuum
- Extremely low growth temperatures < 500°C
- In situ analysis of growing film
- As and, in particular, Ph dopants difficult. Often Sb for n+
Applications of Si epitaxy

**HT epitaxy:**
p- epi on p+ bulk in CMOS for suppression of latch-up
n- on n+ buried collector layer in bipolar devices for reduced series resistance
(single- or double epi):

Problem: *Pattern shift* during n-epi on buried layer

**FIGURE 19**
Schematic illustrations of (a) pattern shift, (b) pattern distortion, and (c) pattern washout. *(After Wolf and Tauber, Ref. 24.)*

Important to control for wafer alignment on buried layer!
LT epitaxy:
SiGe epi for base in bipolars, channel for MOS
Example: KTH SiGe HBT using NSEG SiGe

Grahn et al SSE’00

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<thead>
<tr>
<th>Depth (nm)</th>
<th>Concentration (cm⁻³)</th>
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<td>10¹³</td>
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Oxide
Si3N4
X-base
LOCOS
Aluminum
TiW
TEOS
IDP poly
SiGe epi

Grahn et al SSE’00
SiGe LT epitaxy

Typically at 550-650°C using UHVCVD, LPCVD or APCVD

Selective or non-selective growth

Figure 4. SIMS profile of a SiGe layer capped with a Si layer, grown at 625°C by APCVD. The Ge transitions at the SiGe/Si interfaces are exceptionally steep and totally determined by the SIMS resolution.

Figure 7. SIMS profiles of an HBT structure grown by APCVD at 900°C (collector) and 700°C (base and emitter). The box-shaped profiles allow very accurate control of the base width and dopant content. The As signal in the SiGe material is meaningless due to interference of As and GeH.

de Boer MRS 94
Si SEG
Conventional chemistry:

Addition of HCl to DCS makes Si epi selective with respect to field oxide
SEG is a difficult process in VLSI!
STI isolation is the preferred process choice

FIGURE 25
Schematic illustration of a typical SEG process for device isolation:
(a) oxide deposition; (b) window formation; (c) epi growth; (d) n-well drive-in. (After Borland and Drowley, Ref. 57.)
SiGe SEG

Selective epitaxial growth (SEG) of SiGe in a double-poly bipolar process

SiGe is self-aligned to the base poly overhang

Infineon B7HF (Meister IEDM '95)
Advanced LT epitaxy

Epitaxial lateral overgrowth (ELO)

Adding methylsilane ($\text{CH}_3\text{SiH}_3$) to SiGe epitaxy for SiGeC HBTs

Examples:

Si npn using LTE base + ELO for base poly

From J. Burghartz, IBM

Fig. 1 SEEW process flow for NPN transistors.
SiGe (C) HBT using SEGcollector and NSEG
SiGe(C)

Si CMP intermediate step between SEG and NSEG

On-going KTH research project together with MIC